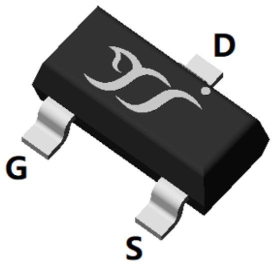
YJL3404A

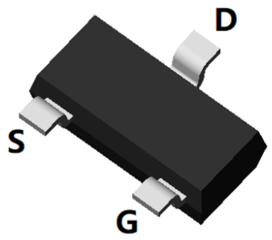
RoHS
COMPLIANT

RECOMMEND
YJL3404B
FOR NEW DESIGN

N-Channel Enhancement Mode Field Effect Transistor

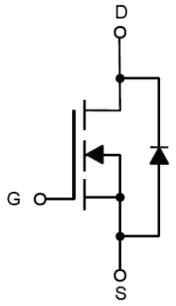


Top View



Bottom View

SOT-23



Product Summary

● V_{DS}	30V
● I_D	5.6A
● $R_{DS(ON)}$(at V_{GS}=10V)	＜24mohm
● $R_{DS(ON)}$(at V_{GS}=4.5V)	＜38mohm

General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	5.6	A
	T_A=70℃		4.5	
Pulsed Drain Current [A]		I_{DM}	30	A
Total Power Dissipation	T_A=25℃	P_D	1.2	W
	T_A=70℃		0.8	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	104	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3404A	F2	R4.	3000	30000	120000	7“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS1}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1	1.5	2.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=5.6A		17	24	mΩ
		V_{GS}=4.5V, I_D=5A		26	38	
Diode Forward Voltage	V_{SD}	I_S=5.6A,V_{GS}=0V			1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V,f=1MHZ		526		pF
Output Capacitance	C_{oss}			78		
Reverse Transfer Capacitance	C_{rss}			69		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=15V,I_D=5.6A		12.22		nC
Gate-Source Charge	Q_{gs}			2.37		
Gate-Drain Charge	Q_{gd}			2.31		
Reverse Recovery Chrage	Q_{rr}	I_F=5.6A, di/dt=100A/us		1.28		
Reverse Recovery Time	t_{rr}			16.5		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DS}=15V, I_D=5.6A R_{GEN}=3Ω		5		
Turn-on Rise Time	t_r			28.2		
Turn-off Delay Time	$t_{D(off)}$			12.8		
Turn-off fall Time	t_f			21.6		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{θJA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{θJC}$ is guaranteed by design, while $R_{θJA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

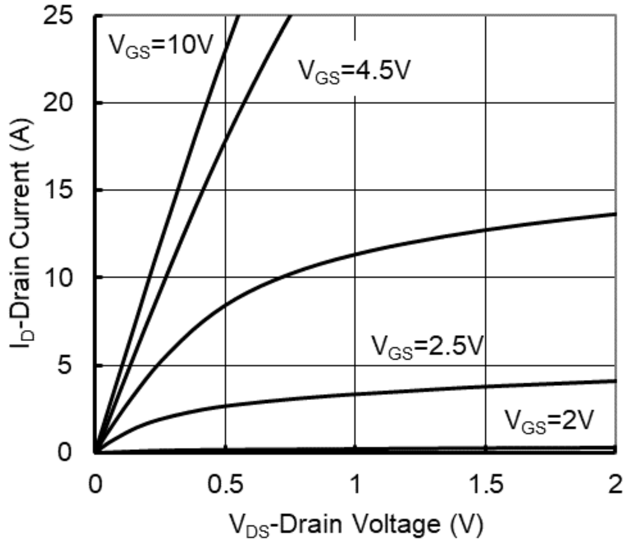


Figure1. Output Characteristics

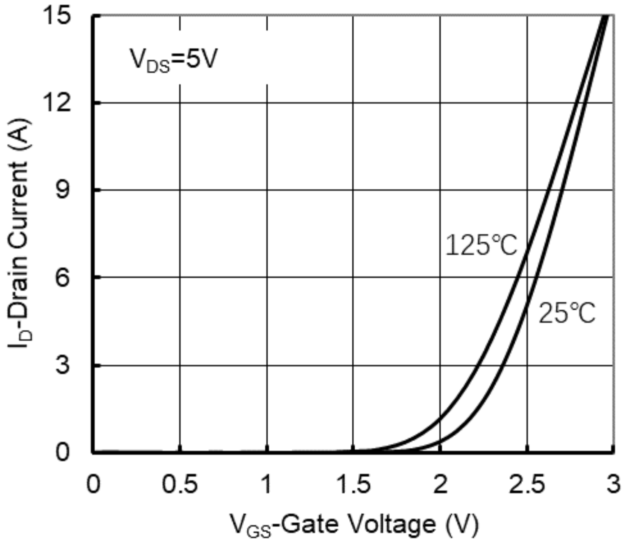


Figure2. Transfer Characteristics

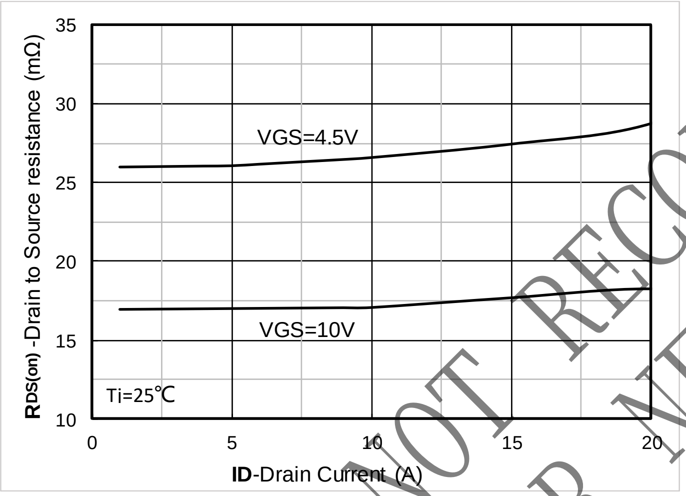


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

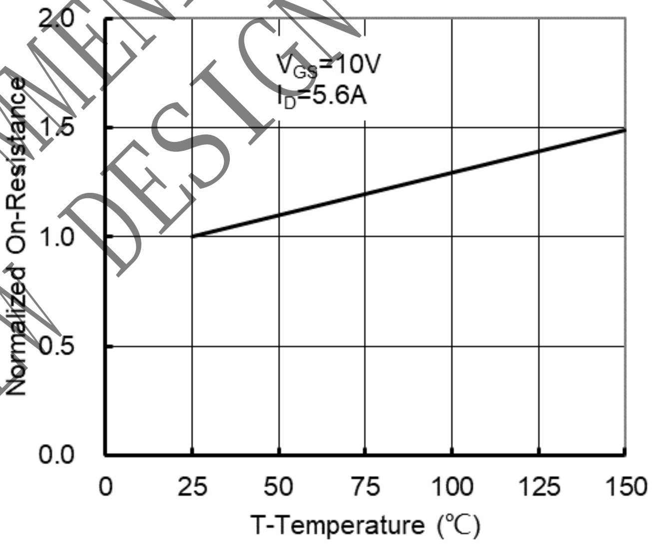


Figure 4: On-Resistance vs. Junction Temperature

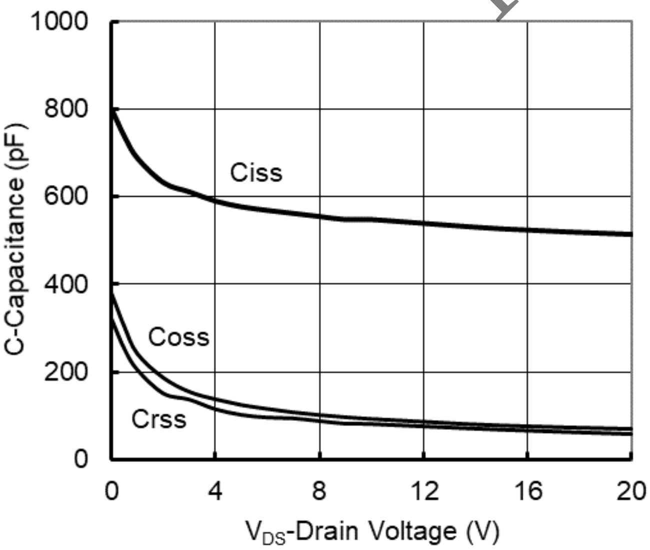


Figure5. Capacitance Characteristics

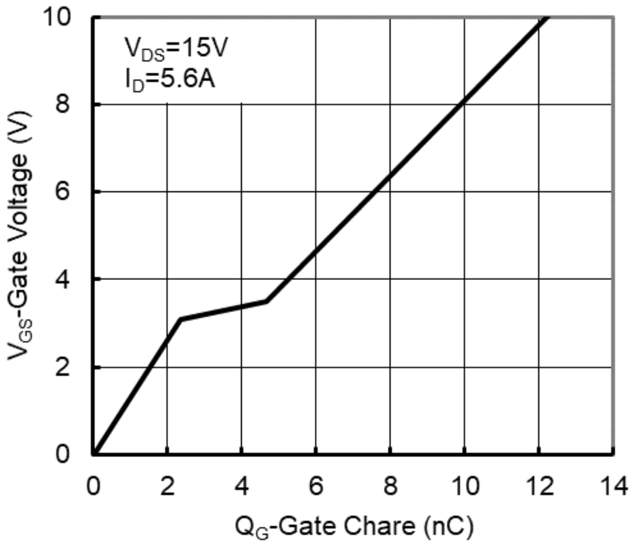


Figure6. Gate Charge

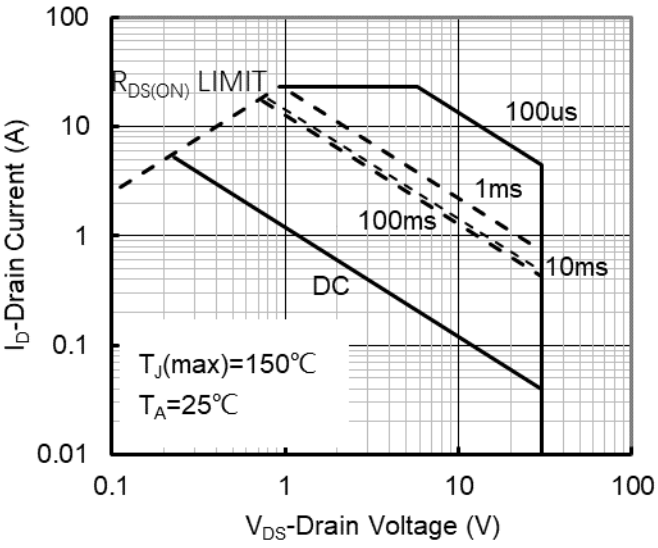


Figure7. Safe Operation Area

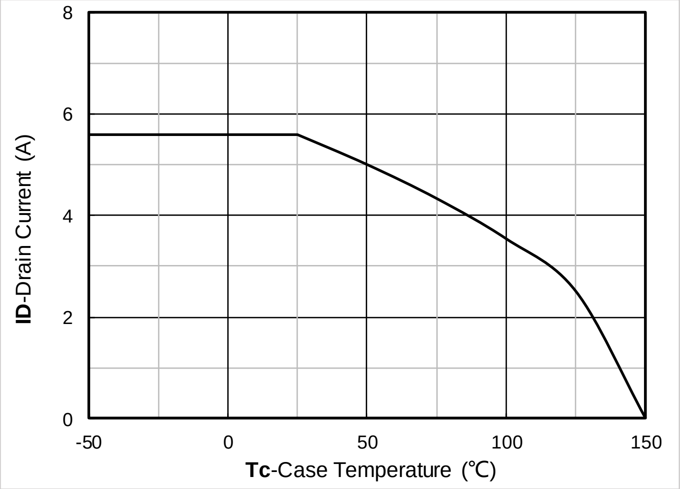


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

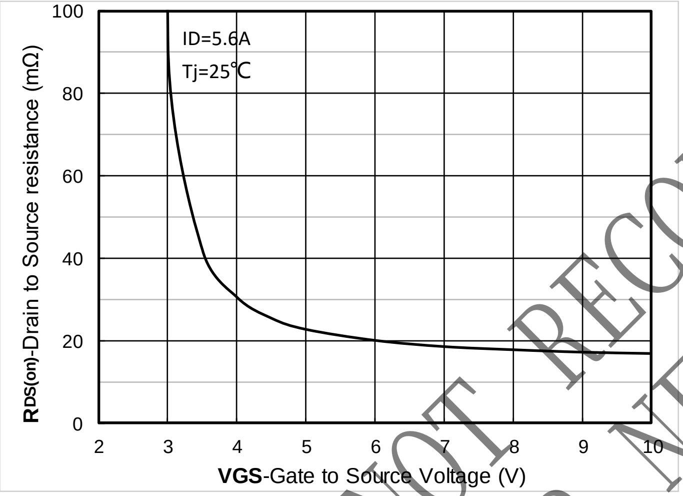


Figure 9. On-Resistance vs Gate to Source Voltage

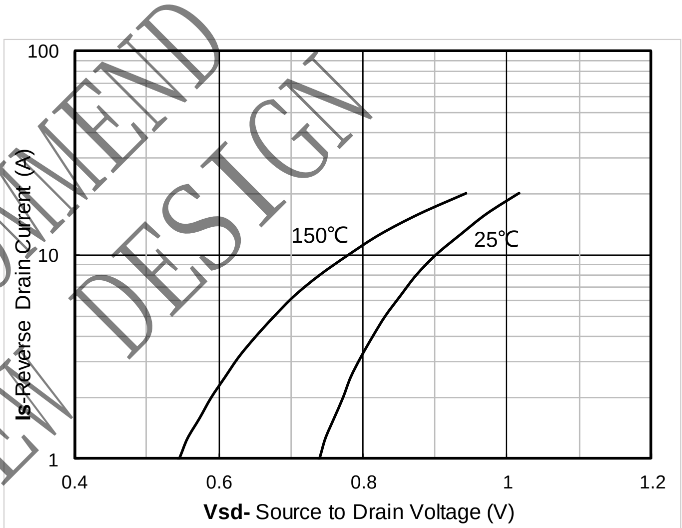


Figure 10. Forward characteristics of reverse diode

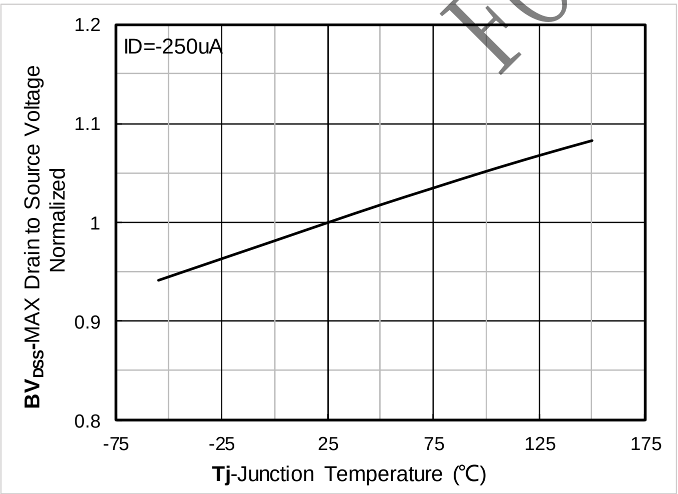


Figure 11. Normalized breakdown voltage

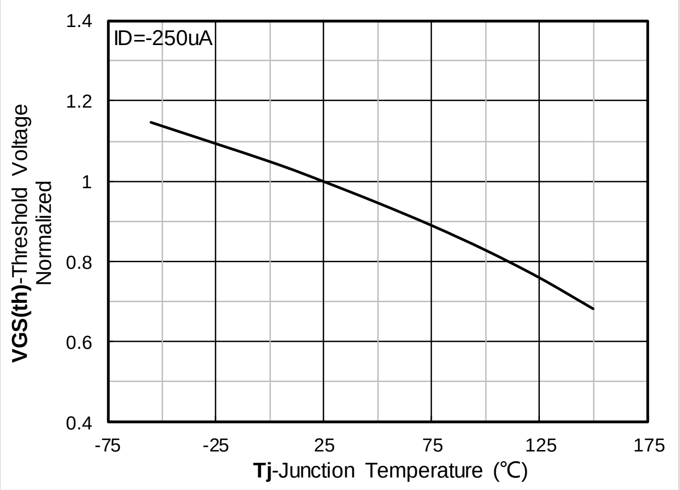


Figure 12. Normalized Threshold voltage

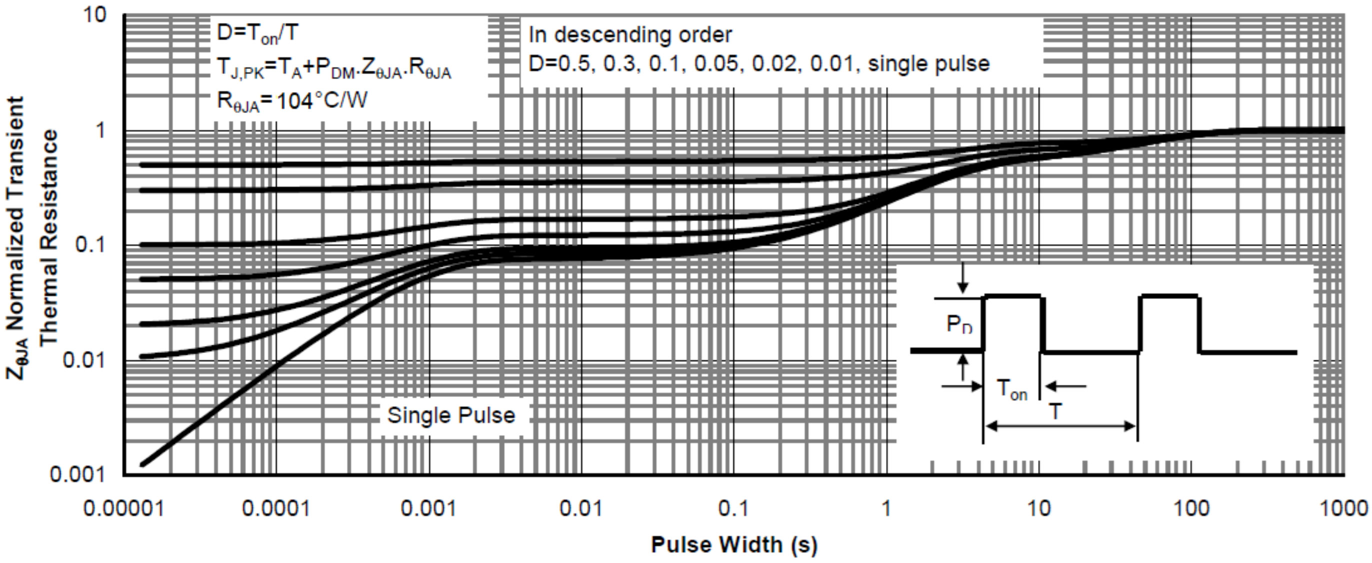
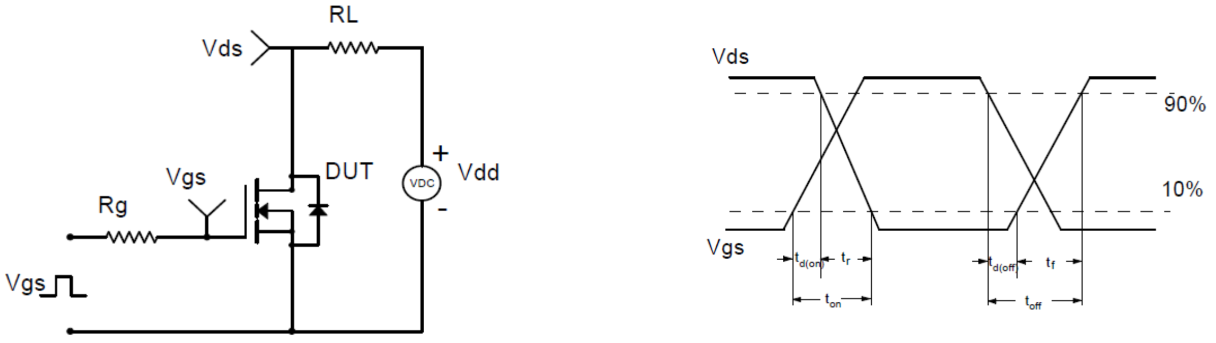
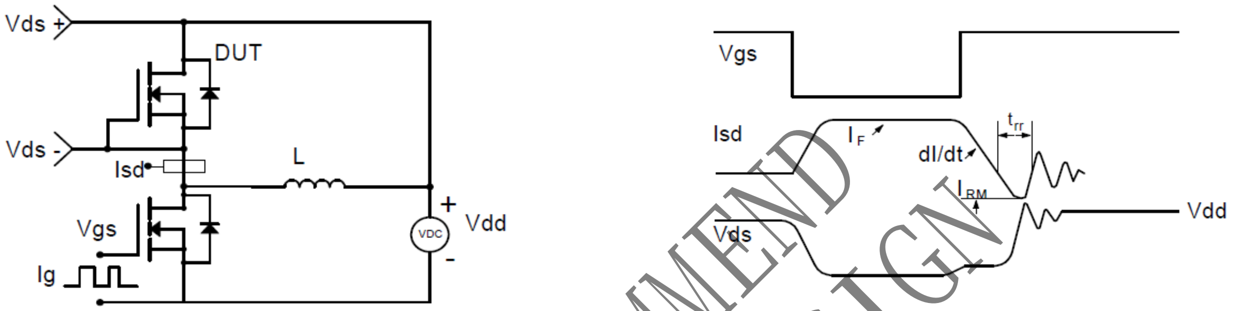


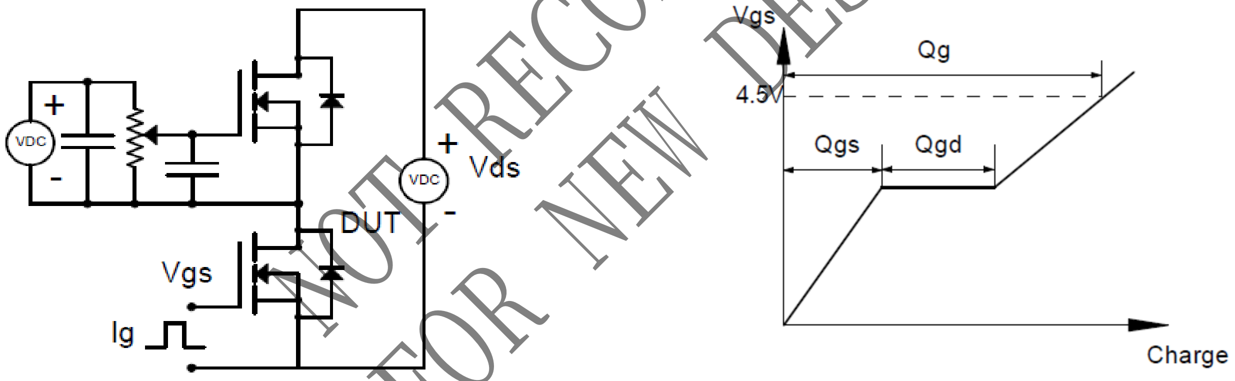
Figure13. Normalized Maximum Transient Thermal Impedance



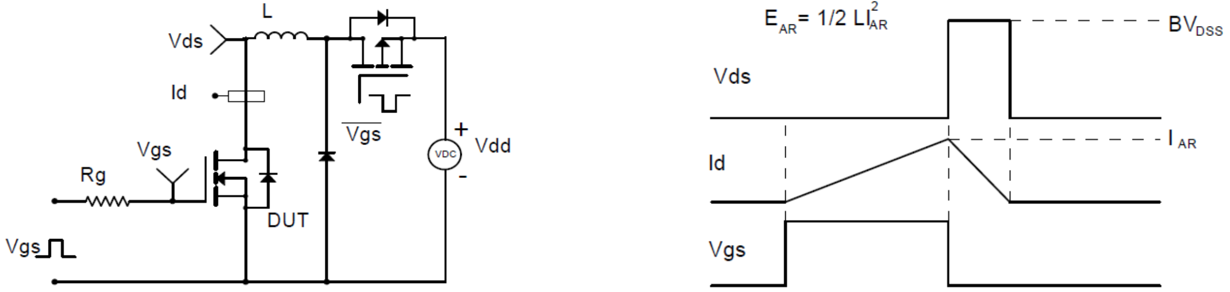
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

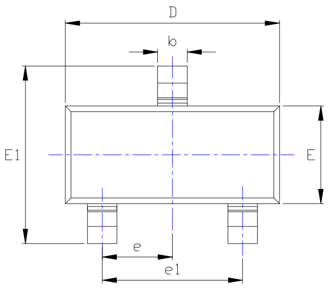


Gate Charge Test Circuit & Waveform

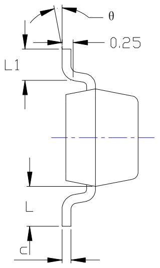


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

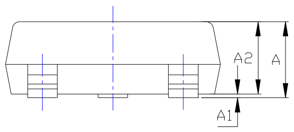
■ SOT-23 Package information



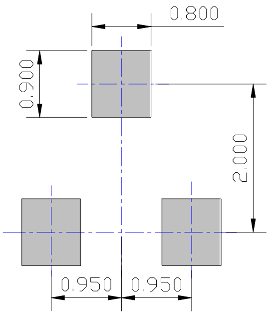
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT：mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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